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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,634	04/07/2005	Jurgen Holz	10808/231	7531

48581 7590 10/04/2007

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EXAMINER	
CRUZ, LESLIE PILAR	
ART UNIT	**PAPER NUMBER**
2826	

MAIL DATE	DELIVERY MODE
10/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/530,634	HOLZ ET AL.	
	Examiner	Art Unit	
	Leslie P. Cruz	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-9 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-9 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 30 August 2007 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 23 and 24 recites the limitation "spacer" in line 2 of claim 23 and line 2 of claim 24. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9, 5, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Roberds (US 6,399,973 B1).

With respect to claim 9, Roberds (Figs. 1-6) discloses a field-effect transistor with local source-drain insulation, having a semiconductor substrate [16]; a source depression [30a] and a drain depression [30b], which are formed in a manner spaced apart from one another in the semiconductor substrate, wherein the source and drain depressions have, in an upper region, a widening [28a, 28b] with a predetermined depth for realizing defined channel connection regions [28]; a depression insulation layer [21a, 21b], which is formed at least in a bottom region of the source depression and of the drain depression, wherein the depression insulation layer has a depression sidewall insulation layer, which is formed in a sidewall region of the source and drain depressions but does not touch the gate dielectric; an electrically conductive filling layer [40a, 40b], which is formed for realizing source and drain regions and for filling the source and drain depressions at a surface of the depression insulation layer, wherein the electrically conductive filling layer has a seed layer [column 6 lines 11-12] for improving a deposition in the source and drain depressions, the seed layer comprising silicon; a gate dielectric [14], which is formed at a substrate surface between the source and drain depressions; and a gate layer [12], which is formed at a surface of the gate dielectric, wherein the depression sidewall insulation layer extends into a region below the gate dielectric.

With respect to claim 5, Roberds discloses the field-effect transistor as claimed in claim 9. Roberds (Figs. 1-6) further discloses a gate insulation layer [22] is formed at sidewalls of the gate layer [12].

With respect to claim 6, Roberds discloses the field-effect transistor as claimed in claim 9. Roberds (Figs. 1-6) further discloses the field-effect transistor is bounded by shallow trench isolations [18].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberds.

With respect to claims 7 and 8, Roberds discloses the field-effect transistor as claimed in claim 9. Roberds does not disclose that the field-effect transistor has lateral structures < 100 nm or that the source and drain depressions have a depth of approximately 50 nm to 300 nm. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the field-effect transistor of Roberds to have lateral structures < 100 nm or the source and drain depressions have a depth of approximately 50 nm to 300 nm in order to miniaturize the device while suppressing the resistance. The specific claimed relative dimensions of the lateral structures or the source and drain depressions, absent any criticality, are only considered to be the "optimum" dimensions that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired adhesive strength, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained.

Accordingly, since the applicants have not established the criticality (see next paragraph below) of the stated relative thicknesses, it would have been obvious to one of ordinary skill in the art to use these values in the device of Roberds.

The specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, claims 7 and 8 are not patentably distinguishable over the Roberds reference.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roberds in view of Murthy et al. (US 2003/0080361 A1).

With respect to claim 22, Roberds discloses the field-effect transistor as claimed in claim 2. Roberds (Figs. 1-6) discloses a gate insulation layer [22] is formed at sidewalls of the gate layer. Roberds does not specify that a spacer [26] is located laterally between the gate insulation layer and the depression sidewall insulation layer. However, Murthy et al. (Fig. 6) discloses that it is well known for a spacer [see figure below] to be located laterally between the gate insulation layer [see figure below] and the depression sidewall insulation layer [38]. It is well known for a spacer to be located laterally between the gate insulation layer and the depression sidewall insulation layer in order to further protect the gate electrode. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the device of Roberds to have a spacer located laterally between the gate insulation layer and the depression

sidewall insulation layer, such as taught by Murthy et al. in order to further protect the gate electrode.

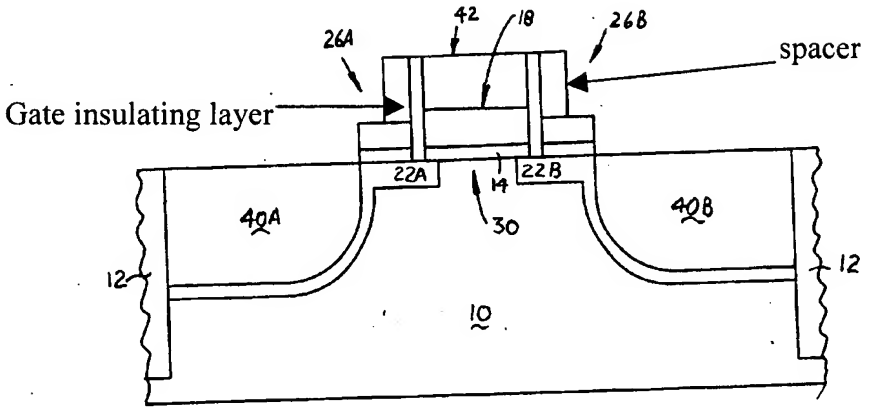

FIG 6

Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberds in view of Murthy et al. (US 2002/0190284 A1), hereinafter Murthy.

With respect to claim 23, Roberds discloses the field-effect transistor as claimed in claim 2. Roberds does not specify that a spacer comprises silicon nitride. Murthy (Figs. 8-14) discloses that it is well known for a spacer [326] to comprise silicon nitride [paragraph 0050]. It is beneficial for the spacer to comprise silicon nitride because of its resistance to wet etching steps. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the device of Roberds to comprise a spacer that comprises silicon nitride such as taught by Murthy, because of its resistance to wet etching steps.

With respect to claim 24, Roberds discloses the field-effect transistor as claimed in claim 2. Roberds does not disclose that a spacer extends into the widening. Murthy (Figs. 2, 8-14) discloses that it is well known for a field-effect transistor to comprise a spacer [213] that extends

into the widening [244]. Murthy teaches that it is beneficial for a spacer to extend into the widening in order to further reduce the distance between the gate electrode and the electrically conductive filling layer, which would reduce an adverse capacitance [paragraph 0030]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made for a spacer to extend into the widening in order to further reduce the distance between the gate electrode and the electrically conductive filling layer which would reduce an adverse capacitance.

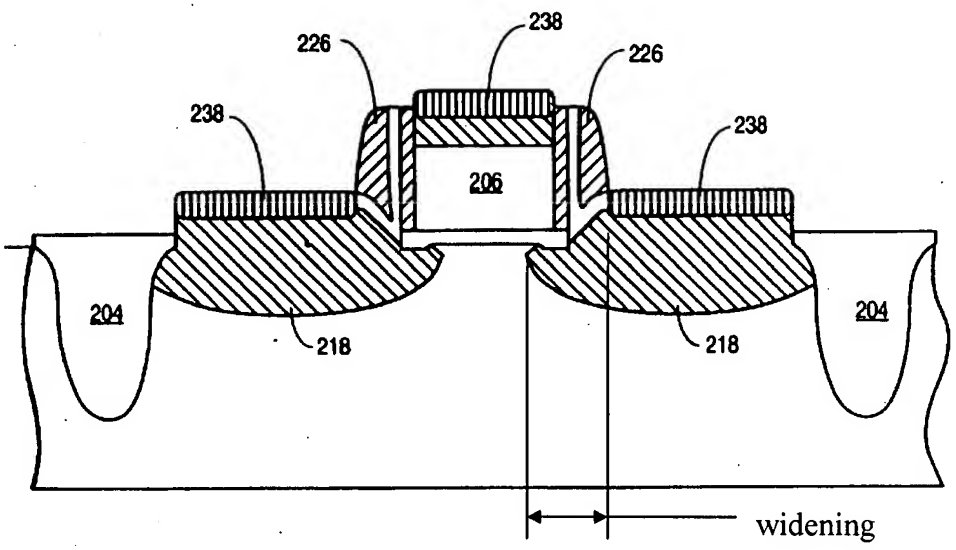

FIG. 13

Response to Arguments

Applicant's arguments filed 18 July 2007 have been fully considered but they are not persuasive. Applicants argue Roberds (US 6,399,973 B1) does not teach or suggest each and every element of the present invention according to claim 9. Specifically, Applicants argue the

depression sidewall insulation layers (21a, 21b) or Roberds extend adjacent to but not into the region below the gate insulation layer. However, Figs. 1-6 of Roberds teaches the depression sidewall layers [21a, 21b] extends into a region below the gate dielectric. Claim 9 does not distinguish over the Roberds reference because it does not recite the depression sidewall layers overlaps with the gate dielectric.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Telephone/Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leslie P. Cruz whose telephone number is 571-272-8599. The examiner can normally be reached on Monday-Friday 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisors, Sue A. Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

lpc

Leslie Pilar Cruz
Examiner
Art Unit 2826